BROADCOM Release Notes: Point Release: CtrlFw_Ph_26.0_Point_Generic - 26.00.01.00 Firmware

ReleaseOrder ID:	*DCSG01496991*
Headline:	*Point Release: CtrlFw_Ph_26.0_Point_Generic - 26.00.01.00 Firmware*
Release Version:	*26.00.01.00*
UCM Project:	*CtrlFw*
Sub UCM Project:	*CtrlFw_Ph_26.0_Point_Generic*
UCM Stream:	*CtrlFw_Ph_26.0_Point_Generic*
Release Type:	*Point*
State:	*Open*
Release Baseline:	*CtrlFw_Ph_26.0_Point_Generic-2023-05-24-26.00.01.00_REL_1684917870@ \SAS35*
Release Date:	*2023-05-24 08:43:31.000000*
Date Generated:	*May 24, 2023*

GCA Release Advisory

- **Release Advisory From ReleaseOrder DCSG01496991 (Point Release: CtrlFw_Ph_26.0_Point_Generic - 26.00.01.00 Firmware):**

Defects Fixed (1):

ID: DCSG01494193 (Port Of Defect DCSG01451450)

Headline: [95xx]: Incorrect slot number management for non-UBM backplanes

Description Of Change: - Defined a field Slotx1 in the CONTROLLER_PHY structure, and initialized it with phy x1 configuration.
- Use Slotx1 to obtain the slot numbers for phys linked up to SAS or if nothing is attached or if phy has PCIe enabled with link width x1 configured.
- Update the Slot field based on the link width configuration for non-UBM backplanes.
- While obtaining the Slot number for the controller Phy for no backplane case, do not check if it is a non-SGPIO managed Phy. Because firmware defaults vSES LED management of all controller Phy attached to SGPIO, therefore this check will never pass.

Issue Description: CONTROLLER_PHY structure does not have a field defined for Slotx1, field Slot is used instead. The field Slot follows x1/x2/x4 slot numbering based on the NVDATA and link width, and the field Slotx1 is initialized with phy x1 configuration.
Current firmware updates the field Slot for non-UBM backplanes based on the x1 slot numbers as programmed in the NVDATA instead of using link width. Due to this unique slot numbers are assigned for the phys configured with link width more than x1.

If I2C backplane detection fails and NVData is configured to enable NVMe drive detection on backplane detection failure, controller firmware is assigning slot numbers to controller Phys based on the link width configured in PCIe IO Unit Page 1.
But while obtaining the slot numbers for NVMe attached phys based on link width, firmware has a check if this Phy is non-SGPIO managed. Since firmware defaults vSES LED management of all controller Phy attached to SGPIO, so this check was failing and X1 slot number was assigned for NVMe phys instead of assigning based on the link width.

Steps To Reproduce: Connect M.2 controller and load 7.25 and see that slot numbers are 0 and 4